WHAT IS CLAIMED IS:

1. A method for processing integrated circuit devices, the method comprising:

providing a monitor wafer, the monitor wafer comprising a silicon material;

introducing a plurality of particles within a depth of the silicon material, whereupon the plurality of particles cause the silicon material to be in an amorphous state;

introducing a plurality of dopant particles into a selected depth of the silicon material using an implantation tool, the amorphous state trapping the dopant particles;

subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant;

removing the monitor wafer;

measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer;

determining a dose of the dopant bearing impurities; and

operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor water is within a tolerance of a specification limit.

2. The method of claim 1 wherein the monitor wafer is substantially free of screen oxide overlying a surface of the monitor wafer.

3. The method of claim 1 wherein the plurality of particles are silicon bearing impurities.

4. The method of claim 3 wherein the silicon bearing impurities are implanted using a dose of 1 X 10^{15} atoms/cm^2 and an energy of 20 keV.

5. The method of claim 1 wherein the dopant particles are boron bearing impurities.

6. The method of claim 5 wherein the boron bearing impurities are implanted using a dose ranging from about 5 X10^{13} through 4 X 10^{14} atoms/cm^2 and an energy ranging from about 1-2 keV.

7. The method of claim 1 wherein the thermal anneal process is an RTP process at about 700 Degrees Celsius.

8. The method of claim 1 wherein the thermal anneal process is an RTP process ranging from about 650 to 750 Degrees Celsius.

9. The method of claim 1 wherein the thermal anneal process is a rapid thermal anneal process.

10. The method of claim 1 wherein the sheet resistivity is provided in a separate tool.

11. The method of claim 1 wherein the operating of the production wafers occurs for 24 hours after determining the dose of the dopant impurities.

12. The method of claim 1 wherein the thermal anneal process also recrystallizes a portion of the amorphous silicon.

13. A method for processing semiconductor waters, the method comprising:

providing a monitor wafer, the monitor wafer comprising a crystalline material;

introducing a plurality of particles within a depth of the material, whereupon the plurality of particles cause the crystalline material to be in an amorphous state;

introducing a plurality of dopant particles into a selected depth of the crystalline material in the amorphous state using an implantation tool, the amorphous state trapping the dopant particles;

subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant;

removing the monitor wafer;

measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer;

determining a dose of the dopant bearing impurities; and

operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor water is within a tolerance of a specification limit.

13. The method of claim 12 wherein the crystalline material comprises silicon.

14. The method of claim 12 wherein the dose of the dopant bearing impurities is determined using a relationship between resistivity values and dose values.

15. The method of claim 14 wherein the relationship has been provided in a spatial plot.

16. The method of claim 12 wherein the plurality of particles comprise silicon bearing particles.

17. The method of claim 12 wherein the dopant bearing impurities comprise boron species.

18. The method of claim 11 wherein the monitor water is substantially free from an overlying oxide layer before introducing the dopant bearing impurities.

19. The method of claim 11 wherein the monitor wafer is silicon wafer.

20. The method of claim 11 wherein the one or more production wafers is characterized by a shallow junction depth of less than about 40 nm.